MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2018/2019

TAO1221 – COMPUTER ARCHITECTURE AND ORGANISATION

(All sections / Groups)

27 MAY 2019
2.30 p.m. – 4.30 p.m.
(2 hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 6 pages including cover page with 5 Questions only.
2. Attempt **ALL** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please print all your answers in the Answer Booklet provided.

QUESTION 1

(a) List the evolution of computer architecture from First Generation until Later Generation. [2 marks]

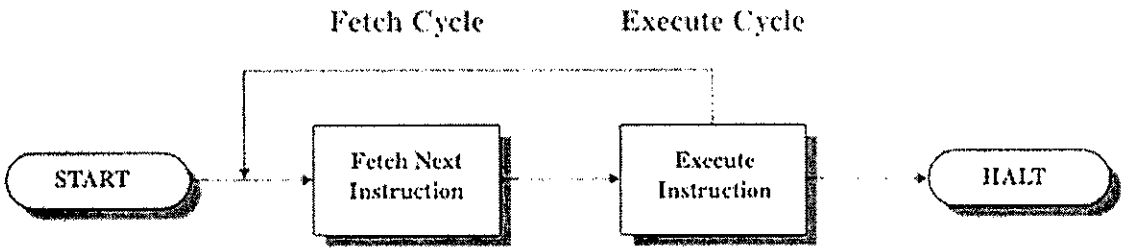
(b) State **THREE (3)** characteristics of Second Generation Computers. [1.5 marks]

(c) Describe the content of Memory Address Register (MAR), Memory Buffer Register (MBR), Instruction Register (IR), and Program Counter (PC). [2 marks]

(d) Discuss **THREE (3)** key concepts of von Neumann architecture. [1.5 marks]

(e) (i) Discuss **TWO (2)** approaches to deal with multiple interrupts. [2 marks]

(ii) Redraw the diagram below to include the interrupt cycle. [1 mark]



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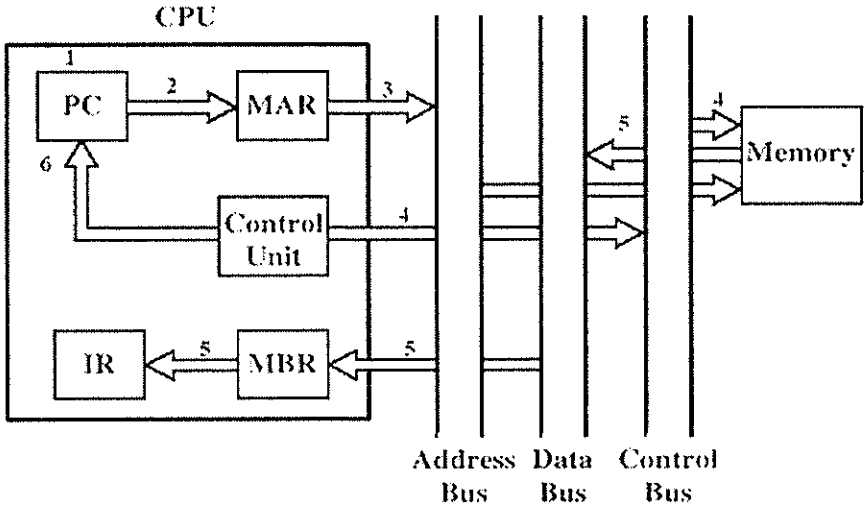
QUESTION 2

(a) From the following data flow diagram, describe the **SIX (6)** processes during Fetch Cycle. [3 marks]



(b) Briefly discuss **THREE (3)** types of pipeline hazards. [3 marks]

(c) Explain **TWO (2)** basic tasks performed by a control unit. [2 marks]

(d) Write the micro-operations of an execute cycle to add the contents of location X to register R1 (ADD R1, X) in the form of symbolic sequence of events; assuming IR contains ADD instruction and t_1, t_2, t_3 are successive time units. [2 marks]

Continued ....

QUESTION 3

(a) Determine the range of an 8-bit two's complement representation. [1 mark]

(b) Calculate the output and determine the overflow status for the following arithmetic operations in 4-bit two's complement representation.

i. -6 + 5 [1.5 marks]

ii. -4 – 5 [1.5 marks]

(c) Assume the usage of IEEE 64-bit format for the representation of floating-point number as given below:

0	10000000011	0111010000000000000000000000000000000000000000000000
Sign Bit (1 bit)	Biased Exponent (11 bits)	Normalized Mantissa (52 bits)

Identify the following:

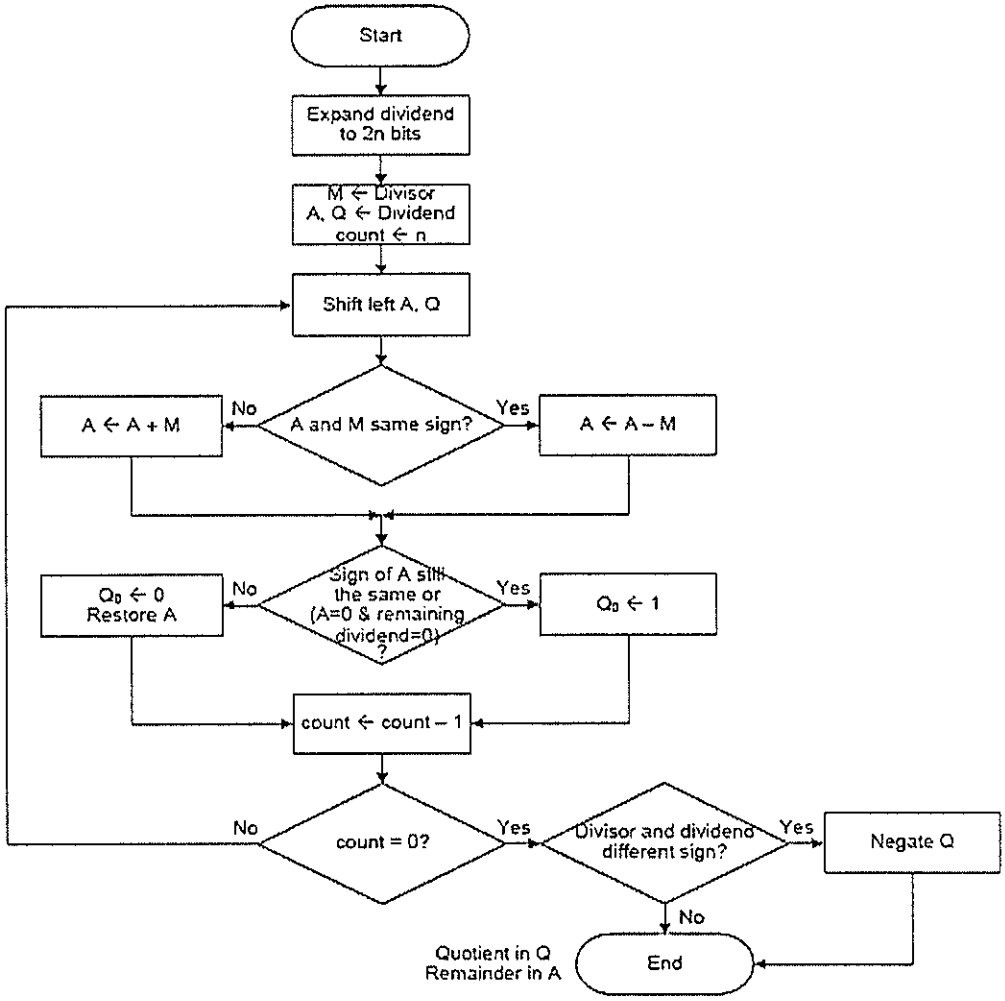
i. Biased exponent value in decimal [0.5 marks]

ii. True exponent value in decimal [0.5 marks]

iii. Decimal equivalent of the given 64-bit floating point number [1 mark]

Continued ....

(d) Given the flowchart for Restoring Division Approach:



Divide (-7) / (2) in binary two's complement notation, using Restoring Division Approach. [4 marks]

Continued ....

QUESTION 4

(a) Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 256-byte line size. Assume a direct mapped cache with a tag field in the address of 14 bits.

i. Show the format of the memory addresses. [2 marks]

ii. Determine the following parameters: [3 marks]
   a. Number of addressable units
   b. Number of blocks in main memory
   c. Number of lines in cache.

(b) Describe **THREE(3)** reasons why transfer of control operations are required in assembly language program. [3 marks]

(c) Describe the register indirect addressing. [2 marks]

QUESTION 5

(a) Describe the meaning of each of the **FOUR (4)** states in the MESI protocol. [4 marks]

(b) Compare the difference between SRAM (Static Random Access Memory) and DRAM (Dynamic Random Access Memory) in term of application. [2 marks]

(c) Describe **FOUR (4)** benefits of clustering. [4 marks]

End of Paper.